REMARKS

Reconsideration and allowance of the subject application are respectfully solicited.

Claims 1, 3, 4, and 6 through 10 are pending, with Claims 1 and 10 being independent. Claims 1 and 10 have been amended.

Claims 1, 3, 4, and 6 through 10 again were variously rejected under 35 U.S.C. § 103 over U.S. Patent Application Publication No. US 2002/0024602 A1 (Juen, et al.), "System on a Chip for a Digital Still Camera" (Okada, et al.), U.S. Patent No. U.S. Patent No. 5,737,014 (Tojo, et al.), U.S. Patent No. 6,603,866 B1 (Motono), U.S. Patent No. 5,262,871 (Wilder, et al.). All rejections are respectfully traversed.

Claim 1 recites, *inter alia*, that the memory interface is capable of generating addresses of a memory of larger capacity, corresponding to a number of pixels greater than the first number of pixels, than the second memory, wherein the converting means, first memory for storing the moving image signal, memory interface, and still image processing means are provided on a single integrated circuit, and the image pickup means and second memory are built as a circuit *different* from the single integrated circuit (with use of a predetermined recording format as claimed).

Claim 10 recites, *inter alia*, that the memory interface is capable of generating addresses of a memory of larger capacity, corresponding to a number of pixels greater than the first number of pixels, than the second memory, wherein the input unit, conversion circuit, first memory for

storing moving image signal, memory interface, and still image processing circuit are provided on a single integrated circuit, and the second memory is built as a circuit *different* from the single integrated circuit (with use of a predetermined recording format as claimed).

Applicant respectfully submits that none of Juen, Okada, et al., Tojo, et al., Motono, and Wilder, et al., even in the proposed combinations, assuming, *arguendo*, that such could be combined, discloses or suggests at least the above-discussed claimed features as recited, *inter alia*, in Claims 1 and 10.

The Official Action acknowledges that Juen fails to show such features, and therefore relies upon Okada, et al. for showing an integrated circuit, stating at page 2 of the Official Action, "in section 3 of Okada the memories are built on the same IC", and stating at page 4 that Okada, et al. shows providing the first memory, a memory interface, conversion means, and still image processing means as a single integrated circuit. Such reliance is respectfully traversed.

Applicant submits that, reviewing Okada, et al.'s Fig. 1, it is apparent that the SDRAM is provided ***separately*** from the ASIC. Turning to the Official Action's reference to Okada, et al.'s Section 3, that section states:

> 3. One-Chip LSI for DSC
>
> This system can process DSC signals by itself because it is integrated with a 32-bit RISC CPU, Motion JPEG, CCD signal processor, CCD driver circuit, video

> encoder DA converter, AD converter, memory controller, **memories**, interface for peripherals, and other devices. (See Figure 1 for block diagram.) The main technologies developed for the system are as follows

Also, there is a reference to a 2KByte data memory at the bottom right of page 586 of Okada, et al. And there is a reference to a "Line Memory x4" in Fig. 3. However, Applicant respectfully submits that there is simply *no indication* in Okada, et al. that the "memories" relied upon in Okada, et al. section 3 are the specific memories recited in the claims. Indeed, that section of Okada, et al. states "(See Figure 1 for block diagram.)", and, as discussed above, Okada, et al.'s Fig. 1 is silent as to the claimed features. Therefore, Applicant respectfully traverses the reliance upon Okada, et al.'s section 3.

The Official Action acknowledges deficiencies of Juen and Okada, et al. and therefore relies upon Tojo, et al.'s memory 7. This reliance is traversed. Tojo, et al. states that memory is limited and that it may be possible in the future to store several tens of frames or more (see col. 5, ll. 56-60), but Applicant submits that such merely refers to increase of memory capacity and provides no suggestion of the above-discussed claimed features including the feature of the capacity corresponding to a number of pixels greater than the first number of pixels, etc. Also, Applicant submits that Tojo, et al. does not disclose both still and moving image capture, as a result of which there is no teaching, motivation, or suggestion to combine Tojo, et al. with Juen.

It is further respectfully submitted that there has been no showing of any indication of motivation in the cited documents that would lead one having ordinary skill in the art to arrive at the above-discussed claimed features. Applicant submits that by means of said features, even if the number of pixels of a still image signal increases so that a memory having larger storage capacity is required as the second memory, the apparatus of the present invention can still process the still image signal without changing the configuration of the single integrated circuit, since the memory interface is arranged so as to generate addresses of a memory of larger capacity than the second memory.

The dependent claims are also submitted to be patentable because they set forth additional aspects of the present invention and are dependent from independent claims discussed above. Therefore, separate and individual consideration of each dependent claim is respectfully requested.

Applicant submits that this application is in condition for allowance, and a Notice of Allowance is respectfully requested.

Applicant's undersigned attorney may be reached in our Washington, D.C. office by telephone at (202) 530-1010. All correspondence should to be directed to our below listed address.

Respectfully submitted,

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